Development of a Course on High-Speed Digital Circuit Design

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Abstract

To better prepare our electrical engineering students for the challenges posed by advanced digital components, a new course (EECS 713) has been developed at the University of Kansas concerning high-speed digital circuit design for senior- and graduate-level students. For purposes of this course, "high speed" is generally interpreted to mean circuits where the length of the signal's rising or falling edge is greater than about one-fourth of the transmission line length. Course topics include rise and fall times, gate input and output impedance, transmission lines, latency and timing issues, electromagnetic interference, packaging issues, thermal management, terminations and vias, power and ground planes, clock distribution, signal launching, substrate materials, and test and measurement issues. Logic families addressed include CMOS, TTL, ECL, and GaAs. Surface-mount components, routing issues, and passive component characteristics are also addressed. A pseudorandom noise generator and, later, a bit-error rate tester serve as design vehicles for the students to demonstrate their understanding of these topics. Computer-aided design packages are used for design and analysis of multi-layer printed circuit boards.

Introduction

The ever-increasing switching speeds of digital logic devices pose significant challenges for the engineers whose job it is to design systems with these components. The need to prepare engineering students for the challenges awaiting them prompted the development of a new course, High-Speed Digital Circuit Design. While students may have a good understanding of fundamental digital logic design, circuit design, and even transmission line theory, they typically require additional training to combine these skills for designs involving high-speed digital signals. Hence this course attempts to build on this foundation and focuses on the intersection of logic design, microwave engineering, and thermal management.

For purposes of this course, "high-speed" is generally interpreted to mean circuits were the length of the signal's rising or falling edge is greater than about one-fourth of the transmission line length, for it is in these cases where the effects of signal reflections, cross talk, and related phenomena may degrade circuit performance.

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Motivation

The University of Kansas is fortunate to have a high quality microwave engineering component in our EE curriculum complete with a well-equipped teaching laboratory. While many concepts from analog engineering (microwave and radio frequency) are relevant to digital applications, the additional requirements of digital systems require special attention. Examples of additional requirements include signals with spectra that extend from DC to a few GHz, sensitivity to signal level, and timing requirements between various signals having tolerances measured in picoseconds.

Technologies available today enable capabilities that previously were not possible. For example, one gigasample per second (1-GSa/s) analog-to-digital (A/D) converters have made significant impacts in data acquisition systems that have applications in radar systems, test equipment, medical instruments, and communication applications. Similarly 1-GSa/s digital-to-analog (D/A) converters enable the direct digital synthesis of wide bandwidth, custom waveforms which have applications in radar systems, test instruments, and high-end displays. Multigigabit per second (Gb/s) data rates are common in fiber-optic networks requiring high-speed digital circuits in both the transmit and receive subsystems. Finally, multi-GHz processor speeds will require data and address buses with ever-decreasing access times. Unfortunately information on how to successfully apply these technologies was not available in any of our courses.

The motivation behind this course development was not entirely altruistic. Not only do many of our students become employed in industries that use the latest high-speed technologies, a small fraction of them stay to pursue graduate degrees. Knowledge of high-speed digital logic is needed to support our radar systems and remote sensing research, our wireless communications work, and our fiber-optic communication systems projects. From these research projects examples of specific applications and system requirements are readily available for classroom use to demonstrate the relevance of this material.

Course Goals and Outcomes Assessment

The goals for the course are to introduce the student to the considerations and issues of designing circuits for high-frequency analog and digital applications through analytical and simulation techniques.

To assess outcomes, the students should be capable of:

- Describing the characteristics of high-speed digital logic devices
- Selecting appropriate components for and designing high-speed digital circuits
- Designing a multi-layer, printed circuit board suitable for high-speed digital applications
- Discussing the significance of the package technologies related to high-speed digital devices

These objectives are assessed with a final project, mid-term and final examinations, homework assignments, and semester-end course and instructor evaluations completed by the students.

Course Structure

This one-semester (15-week) course is primarily lecture based and has as prerequisites:

- circuits theory and analysis
- electronic circuit theory and analysis
- traveling wave theory and analysis

The course is available for both senior- and graduate-level electrical engineering students. Computer engineering students may be eligible provided they have suitable knowledge of transmission line theory, a topic not currently required in our computer engineering curriculum. Thus far this course has been offered five times with average enrollment of about 18 students, with roughly two-thirds being undergraduates.

Grading is based on the homework assignments, two examinations (mid-term and final), and a final project report with presentation.

The text (H. W. Johnson and M. Graham, *High-Speed Digital Design*[1]) is very appropriate for this course as it provides a thorough coverage of the relevant topics from an application perspective. Many "rules of thumb" are provided, relating specific design parameters to various phenomena. The main disadvantage of this text is the lack of homework exercises. To fill this gap, several miniproject (homework) assignments have been developed that incorporate recent lecture concepts. These assignments were designed to be interrelated so that the final assignment pulls together elements from the previous assignments.

While the text serves as a road map regarding topics relevant to this area, since it is a static reference it cannot incorporate the latest high-speed digital components. To address this facet, and to encourage skills needed for life-long learning, data sheets for the latest high-speed component offerings are obtained via the internet. Numerous links have been compiled and made available to the students providing the latest component information on issues ranging from chip capacitors[2], crystal oscillators[3], ECL[4,5,6] and GaAs[7,8] components, data conversion products[9], and many others. Homework assignments and lecture examples use devices and parameters from these sources.

Other sources with great educational value are the numerous application notes and designer's guides[10,11,12] that many manufacturers in this area generously provide. While most of these sources are long on dos and don’ts and specific design equations while being somewhat short on background theory, the combination of the text with this material provides a very nice treatment of the topic. In addition, the application notes present a teaching opportunity allowing the instructor to justify and provide the rationale behind the various dos and don’ts.

The Miniprojects

A series of homework assignments were developed as miniprojects requiring the application of recent lecture topics. The first assignment reviews the concepts of Thévenin and Norton equivalent circuits, transient response of first-order circuits, and rise times on simple R-C and L-R circuits. Topics discussed during this assignment include the sources and effects of capacitance and inductance, the input and output impedance of digital logic devices, and the frequency content of digital signals.

The second assignment requires the design and analysis of a pseudorandom noise (P/N) generator with length 127 using a shift register and an exclusive-nor gate. This design requires a detailed schematic, timing analysis, a parts list, and the worst-case current requirements. Assumptions given include: all trace lengths are 2 inches (5 cm), board material is FR-4, and the transmission line configuration is stripline. This design is performed for five different technologies including CMOS (National Semiconductor FACT), TTL (Texas Instruments FAST), emitter-coupled logic (ECL) (Fairchild 300 series), and GaAs logic (two varieties, GigaBit Logic and NEC Logic). Data sheets for components from each of these technologies are provided with the assignment. Package options and operating temperatures are specified to minimize the possible operating parameters. Proper termination of the ECL and GaAs circuits is required. The maximum operating frequency under worst-case conditions is determined for each design. In support of this assignment, lecture topics include rise and fall times of various logic technologies, differences in output driver designs, ground bounce and lead inductance, and power dissipation.

Assignment three addresses thermal resistance and device junction temperature. The thermal resistance and junction temperature of transistors in a GaAs die that is dissipating 1.3 W are found for three different substrate materials – LTCC (low-temperture cofired ceramic), LTCC with thermal vias, and aluminum nitride. Thermal properties of semicondutors materials, substrate materials, bonding agents, packaging materials, and forced-air convection cooling with an aluminum heat exchanger (heat sink) are addressed prior to this assignment. Specific details on how to handle thermal vias and heat spreaders are provided in lecture. Thermal and electrical considerations in package design are also discussed, as well as the impact of mismatched thermal coefficients of expansion.

The topic of the fourth assignment is stripline transmission line design. Design equations for stripline from several sources are compared. The effects of manufacturing variations (trace width, substrate thickness, substrate dielectric properties, and metal thickness) on the resultant transmission line impedance are explored. Tolerable impedance variations are found by predicting signal distortion due to reflections in light of the noise margins of the various digital logic technologies. Signal attenuation for specific line lengths and signal frequencies is also determined. Finally the propagation speed, inductance and capacitance per unit length, and minimum acceptable separation for a given crosstalk are determined. Lecture topics supporting this assignment include skin depth, the proximity effect, conductor and dielectric losses,

coupling between transmission lines, the need for continuous reference (ground) planes, and return path current issues.

In the fifth assignment complete bit-error-rate tester (BERT) logic is designed based on information presented by GigaBit Logic[10]. Using two P/N generators, synchronization logic, and error-detection logic are combined in a single design. One P/N generator produces a serial bit pattern for transmission while a matching P/N generator produces a reference pattern to compare the received sequence after an unknown delay in the transmission channel. Figure 1 shows a block diagram of this system. ECL components from Micrel Corp.[4] are specified. In this assignment a complete schematic, multiplayer printed circuit board layout, board stackup, component selection and placement, transmission line design and routing design rules, timing analysis, parts list, and thermal analysis are required. In addition, peer evaluation is also used. Lecture topics supporting this assignment include electromagnetic interference considerations, self-resonance in capacitors, daisy-chain routing, near-end versus far-end terminations, clock fan-out, the importance of matching trace lengths within a data bus, buried and blind vias, and design for testability. Techniques for achieving incremental timing delays are also discussed.

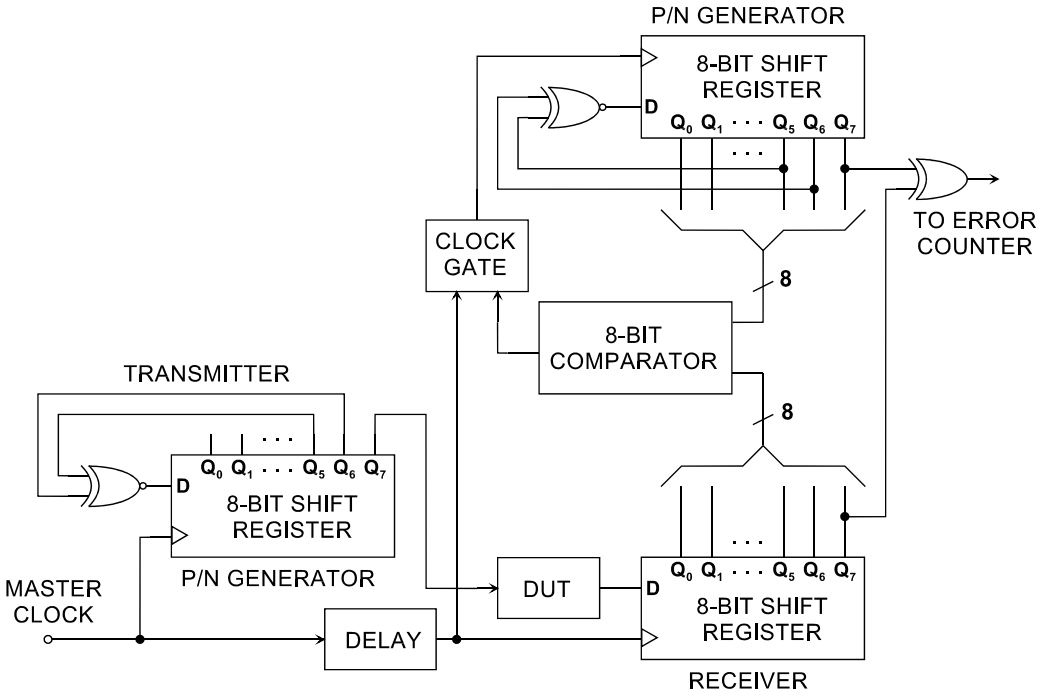

Figure 1. Block diagram of the bit-error-rate tester (BERT).
Adapted from GigaBit Logic[12] p. 8-118.

The objective of the final project is to "demonstrate a working knowledge of high-speed digital design by completing a complex design." On this assignment students may work individually or in teams of two. The topic for the final project is selected by the students in consultation with

the instructor. Project evaluation includes complexity of the topic selected, quality of the presentation, and completeness of the report. Topics have ranged from design of a 200-MSa/s arbitrary waveform generator to exercises for a proposed laboratory to accompany this class to the design of a 1-GSa/s data acquisition system. Topics covered in support of this assignment include pipelining and latency, clock skew, and multiplexing. Presentation skills are also addressed.

Several other topics are covered in the course as well. Trends in integrated circuit technology are discussed including gate delays, the number of pins required for input and output, and the increase in dissipated power. Packaging options discussed include multichip modules, chip-on-board, considerations when using bare die, and wire bonding versus flip-chip technologies. The challenges associated with positive emitter-coupled logic (PECL) are discussed in terms of logic levels and termination requirements. The advantages of differential signal transmission are presented including tolerance to common-mode noise and termination options. Board interconnect options are discussed including shielded ribbon cables with twisted pairs. Electromagnetic emissions regulations and testing requirements are presented as well.

Finally we discuss what we might expect to find in the future. The merits and challenges of optical interconnects between chips are discussed. We also talk about how the extraordinary thermal properties of diamond may play a role in future packaging designs. The challenges associated with chip stacking to achieve exceptional component densities are examined.

Student Feedback

Feedback from the students has generally been very positive regarding this course. The only consistent negative feedback is that the assignments are perceived to be quite time consuming. Positive comments have been received through many situations. In the formal student evaluation of the course and instructor, comments praising the applicability of the course are frequent, particularly the fact that this course couples application with theory. Several students have expressed satisfaction that this course successfully brought together seemingly disparate concepts such as power dissipation, package issues, device impedance, and signal integrity. In particular, the discussion of the current return path provokes "light-bulb moments" in many students, particularly when we trace the different return paths for DC, low- , and high-frequency signal currents. In many instances students will share past design problems that were probably caused by an inadequate current return path.

Several students from this course have taken positions in industry that involve the concepts discussed in this course. Several students now working in the computer design industry, who have stayed in contact with me, have commented on how valuable the concepts covered in this course have been in their daily activities. One student proclaimed with pride that in the first week of his new job, his supervisor asked him to take a look at the Johnson and Graham text saying it contained information relevant to his job assignment. This student was pleased to tell his supervisor that he had not only already read the text, he had taken a course over this material.

Conclusions

A course addressing the intersection of logic design, microwave engineering, and thermal management in support of high-speed digital circuit design has been developed at The University of Kansas for senior- and graduate-level electrical engineering students. A broad range of topics is treated with an emphasis on application, supported by the necessary theory. A series of miniprojects are assigned throughout the course culminating in the design of logic for a rudimentary bit-error-rate tester. The concepts presented in this course have value for students headed for a variety of fields including radar systems, test equipment, computer and communication systems design. Student feedback, both immediate and more retrospective, has been overwhelmingly positive. This course successfully melds circuit design with electromagnetics, digital logic, and mechanical issues including thermal management and package design.

References

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